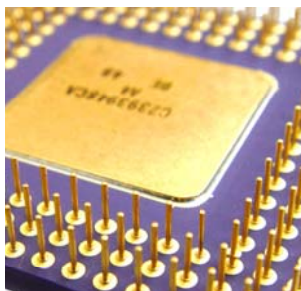


Esterel Technologies' **SCADE Suite Timing Verifier** and **SCADE Suite Stack Verifier**, empowered by Absint aiT/StackAnalyzer, provide software and system designers with an efficient way to automatically analyze and report, at model level, the Worst-Case Execution Time (WCET) and the maximum stack usage of the generated code for your targets. The **SCADE Suite®** model-based development environment is dedicated to design, verification, and generation of critical embedded software that complies with certification standards.



Stack usage analysis and worst case execution time analysis are invaluable to the developers of critical embedded systems and software. In terms of cost efficiency, quality, and safety, developers can no longer rely purely on

manual methods for examining the run-time performance and memory usage of their applications.

Coupling WCET and Stack Analysis with SCADE Suite KCG™-Generated Code

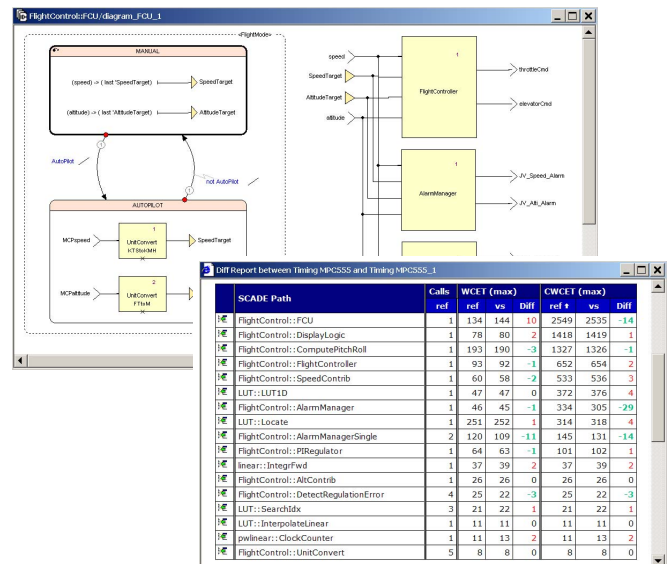
Timing and Stack Verifiers provide SCADE Suite model designers with:

- WCET and stack analyses on code generated by SCADE Suite KCG and results reported back into SCADE Suite design environment
- Single-view representation of several WCET results based on different code generator configurations and analysis sessions

By raising the level of abstraction with model-based development and breakthrough analysis capabilities, embedded software developers can quickly identify and eliminate potential performance bottlenecks and design flaws early in the development cycle.

Product Features

- Estimating WCET and maximum stack size on object code from SCADE Suite models



SCADE Path	calls	ref	ref	vs	Diff	WCET (max)	ref #	CWCET (max)	vs	Diff
FlightControl::FCU	1	134	144	10	2549	2535	-14			
FlightControl::DisplayLogic	1	78	80	2	1418	1419	1			
FlightControl::ComputePitchRoll	1	193	190	-3	1327	1326	-1			
FlightControl::FlightController	1	93	92	-1	652	654	2			
FlightControl::SpeedContrib	1	60	58	-2	533	536	3			
LUT::LUT1D	1	47	47	0	372	376	4			
FlightControl::AlarmManager	1	46	45	-1	334	305	-29			
LUT::Locate	1	251	252	1	314	318	4			
FlightControl::AlarmManagerSingle	2	120	109	-11	145	131	-14			
FlightControl::PRRegulator	1	64	63	-1	101	102	1			
linear::IntegrFwd	1	37	39	2	37	39	2			
FlightControl::AltContrib	1	26	26	0	26	26	0			
FlightControl::DetectRegulationError	4	25	22	-3	25	22	-3			
LUT::SearchIdx	3	21	22	1	21	22	1			
LUT::InterpolateLinear	1	11	11	0	11	11	0			
pwlinear::ClockCounter	1	11	13	2	11	13	2			
FlightControl::UnitConvert	5	8	8	0	8	8	0			

- Fully automated process: code generation from SCADE Suite model, compilation with cross compiler, static analysis, reporting results at SCADE Suite model level. Fully customizable from SCADE Suite or by TCL scripts
- Comparison of analysis sessions and results to easily determine the benefits and costs in time and stack size with regard to the cumulative effect of options from both SCADE Suite KCG Code Generator and the cross compiler



About Timing and Stack Verifier Technology

SCADE Suite Timing Verifier statically computes tight bounds for the Worst-Case Execution Time of tasks in real-time embedded systems. The verification technology directly analyzes binary executables and takes the intrinsic cache and pipeline behavior into account. The precise bound on the execution time enables better system utilization without compromising safety.

Function FlightControl::FCU detail (session Timing MPC555)

**Function FlightControl::FCU detail
(session Timing MPC555)**

FlightControl::FCU Cycle function

Calls: 1
 CWCET (sum): 2549 (63.725 ms) (100.00%)
 WCET (max): 134 (3.35 ms) (5.26%)
 CWCET (max): 2549 (63.725 ms) (100.00%)
 CWCET (avg): 2549.00

FlightControl::FCU Cycle function descendant

SCADE Path	Calls	Kind	Contribution	%
FlightControl::FCU	0	CYCLE	134	5.26
FlightControl::FlightController	1	CYCLE	652	25.58
FlightControl::AlarmManager	1	CYCLE	334	13.10
FlightControl::DisplayLogic	1	CYCLE	1418	55.63
FlightControl::UnitConvert	2	CYCLE	11	0.43

SCADE Suite Stack Verifier automatically calculates the worst-case stack usage of tasks in a program. Underestimating stack usage can lead to serious runtime errors which can be difficult to find. Overestimating stack usage means a waste of memory resources.

ESTEREL Technologies SCADE Suite is the market leading model-based development environment dedicated to critical embedded software. The qualifiable SCADE Suite KCG code generator produces simple C code with all the properties required for critical embedded software:

- **DO-178B** qualified up to level A for Military and Aerospace Industries
- **IEC 61508** certified at SIL 3 by TÜV SÜD for Heavy Equipment, Automotive, and Energy
- **EN 50128** certified at SIL 3/4 by TÜV SÜD for Rail Transportation

Supported Targets

- Supported processor targets for WCET analysis: PowerPC MPC 55xx, MPC 555, MPC 565, MPC 603e, MPC 755s
- Supported processor targets for stack size analysis: all PowerPC

For detailed technical supported platforms, see the Timing and Stack Verifier Supported Platforms Reference Card. For other targets, please contact Esterel Technologies.

Both Verifiers are validated with Wind River®, Green Hills®, and GCC compilers.

Contact Information

Submit questions to Technical Support at support@esterel-technologies.com

Contact one of our Sales representatives at sales@esterel-technologies.com

Direct general questions about Esterel Technologies to info@esterel-technologies.com

Discover the latest news on our products and technology at <http://www.esterel-technologies.com>

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Revision: TSV-TDS-6.1.2 - 17/03/10